

## WHAT IS CLAIMED IS:

1. A method for fabricating a capacitor of a semiconductor device, the method comprising the steps of:

5 (1) forming a first interlayer insulating film on a semiconductor substrate, and then selectively removing the first interlayer insulating film to form a plug contact hole;

(2) forming a first contact plug in the plug contact hole;

10 (3) forming a first barrier layer on an upper surface of a first resultant lamination including the first contact plug, the first resultant lamination having been obtained through steps (1) and (2);

(4) forming a first polysilicon layer and a second barrier layer on the first barrier layer;

(5) sequentially patterning the second barrier layer, the first polysilicon layer, and the first barrier layer, thereby forming a first contact hole which exposes an upper surface of the contact plug;

20 (6) forming a first dielectric layer on an upper surface of a second resultant lamination including the first contact hole, the second resultant lamination having been obtained through steps (1) to (5);

(7) removing portions of the first dielectric layer,

which are located at outside and bottom parts of the first contact hole, thereby leaving a portion of the first dielectric layer located at one side portion of the first contact hole;

5       (8) forming a second polysilicon layer on an upper surface of a third resultant lamination, which has been obtained through steps (1) to (7) and includes the first dielectric layer remaining on said one side portion of the first contact hole, and then removing the second polysilicon  
10 layer located at portions except for the first contact hole;

      (9) forming a second dielectric layer on an upper surface of a fourth resultant lamination obtained through steps (1) to (8), forming a third polysilicon layer on the second dielectric layer, and patterning the third polysilicon  
15 layer;

      (10) forming a second interlayer insulating film on an upper surface of a fifth resultant lamination obtained through steps (1) to (9), and selectively removing the second interlayer insulating film, the patterned third polysilicon  
20 layer, the second dielectric layer, the second barrier layer, and the first polysilicon layer, thereby forming a second contact hole; and

      (11) forming a second contact plug in the second contact hole, and then forming a metal wiring on the second contact

plug and the second interlayer insulating layer.

2. A method for fabricating a capacitor of a semiconductor device as claimed in claim 1, wherein the third polysilicon layer and the first polysilicon layer are connected through the second contact plug.

3. A method for fabricating a capacitor of a semiconductor device as claimed in claim 1, wherein step (7) is performed through a dry-etching process.

4. A method for fabricating a capacitor of a semiconductor device as claimed in claim 1, wherein the first polysilicon layer and the third polysilicon layer are used as an upper electrode.

5. A method for fabricating a capacitor of a semiconductor device, the method comprising the steps of:

(1) forming a first interlayer insulating film on a semiconductor substrate, selectively removing the first interlayer insulating film to form a plug contact hole, and forming a first contact plug in the plug contact hole;

(2) forming a first barrier layer on an upper surface of a first resultant lamination including the first contact plug,

the first resultant lamination having been obtained through step (1);

(3) forming a first polysilicon layer and a second barrier layer on the first barrier layer;

5 (4) forming a second interlayer insulating film on the second barrier layer;

(5) selectively removing the second barrier layer, the second barrier layer, the first polysilicon layer, and the first barrier layer, thereby forming a first contact hole;

10 (6) forming a first dielectric layer on an upper surface of a second resultant lamination including the first contact hole, the second resultant lamination having been obtained through steps (1) to (5);

(7) removing portions of the first dielectric layer, 15 which are located at outside and bottom parts of the first contact hole, thereby leaving a portion of the first dielectric layer located at one side portion of the first contact hole;

(8) forming a second polysilicon layer on an upper 20 surface of a third resultant lamination, which has been obtained through steps (1) to (7) and includes the first dielectric layer remaining on said one side portion of the first contact hole, and then removing the second polysilicon layer located at portions except for the first contact hole;

(9) forming a second dielectric layer on an upper surface of a fourth resultant lamination obtained through steps (1) to (8), forming a third polysilicon layer on the second dielectric layer, and patterning the third polysilicon layer;  
5 layer;

(10) forming a third interlayer insulating film on an upper surface of a fifth resultant lamination obtained through steps (1) to (9), and selectively removing the third interlayer insulating film, the patterned third polysilicon layer, the second dielectric layer, the second interlayer insulating film, the second barrier layer, and the first polysilicon layer, thereby forming a second contact hole; and  
10 layer, the second dielectric layer, the second interlayer insulating film, the second barrier layer, and the first polysilicon layer, thereby forming a second contact hole; and

(11) forming a second contact plug in the second contact hole, and then forming a metal wiring on the second contact plug and the third interlayer insulating layer.  
15 plug and the third interlayer insulating layer.

6. A method for fabricating a capacitor of a semiconductor device as claimed in claim 5, wherein the third polysilicon layer and the first polysilicon layer are connected through the second contact plug.  
20 connected through the second contact plug.

7. A method for fabricating a capacitor of a semiconductor device as claimed in claim 5, wherein step (7) is performed through a dry-etching process.

8. A method for fabricating a capacitor of a semiconductor device as claimed in claim 5, wherein the first polysilicon layer and the third polysilicon layer are used as  
5 an upper electrode.

9. A method for fabricating a capacitor of a semiconductor device as claimed in claim 5, wherein the second interlayer insulating film is formed of an oxide film.

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